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What is claimed is:

1. A flipflop, comprising:

a differential pair comprising a first transistor and a second transistor, wherein control terminals of the first and second transistors are coupled to a first input signal and a second input signal respectively, and first terminals of the first and second transistors are coupled to a common node;

a first latch unit coupled between the common node and a first voltage, and connected to the differential pair in parallel, comprising a first node and a second node to respectively coupled to second terminals of the first and second transistors in the differential pair to generate complementary latch signals according to the first and second input signals;

a signal amplification circuit coupled to the differential pair and the first latch unit, comprising a first control terminal coupled to a control signal, to generate complementary amplified signals according to the complementary latch signals; and

a second latch unit coupled to the signal amplifier circuit to generate complementary static output signals according to the complementary amplified signals and to maintain the

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complementary static output signals, wherein the first input signal is the inverse of the second input signal.

2. The flipflop as claimed in Claim 1, wherein the signal amplification circuit further comprises second and third control terminals coupled to the first input signal and the second input signal respectively.

3. The flipflop as claimed in Claim 2, wherein the first latch unit comprises:

a first inverter comprising an input terminal coupled to the second node, and an output terminal; and

a second inverter cross-coupled to the first inverter, comprising an input terminal coupled to the first node and the output terminal of the first inverter, and an output terminal coupled to the output terminal of the first inverter and the second node.

4. The flipflop as claimed in Claim 2, further comprising a current source transistor coupled between the common node and a second voltage, and comprising a control terminal coupled to the control signal.

5. The flipflop as claimed in Claim 4, wherein the differential circuit further comprises:

a third transistor coupled between the first voltage and the first node comprising a control terminal coupled to the control signal; and

a fourth transistor coupled between the first voltage and the second node comprising a control terminal coupled to the control signal.

6. The flipflop as claimed in Claim 5, wherein the second latch unit comprises:

a third inverter comprising an input terminal and an output terminal; and

a fourth inverter cross-coupled to the fourth inverter, comprising an input terminal and an output terminal coupled to the output terminal and the input terminal of the third inverter respectively, wherein the input terminals of the third and fourth inverters are coupled to the complementary amplified signals respectively.

7. The flipflop as claimed in Claim 6, wherein the signal amplification circuit comprises:

a fifth inverter coupled to the first voltage and comprising an input terminal coupled to the first node;

a fifth transistor comprising a first terminal coupled to the fifth inverter, a control terminal coupled to the control terminal of the second transistor, and a second terminal;

a sixth transistor comprising a first terminal coupled to the second terminal of the fifth transistor, a second terminal coupled to the second voltage, and a control terminal coupled to the control signal;

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a sixth inverter coupled to the first voltage and comprising an input terminal coupled to the second node;

a seventh transistor comprising a first terminal coupled to the sixth inverter, a control terminal coupled to the control terminal of the first transistor, and a second terminal; and

an eighth transistor comprising a first terminal coupled to the second terminal of the seventh transistor, a control terminal coupled to the control signal, and a second terminal coupled to the second voltage.

8. The flipflop as claimed in Claim 6, wherein the signal amplification circuit comprises:

a fifth transistor comprising a first terminal coupled to the first voltage, a control terminal coupled to first node, and a second terminal;

a sixth transistor comprising a first terminal coupled to the second terminal of the fifth transistor, a control terminal coupled to the control terminal of the second transistor, and a second terminal;

a seventh transistor comprising a first terminal coupled to the second terminal of the sixth transistor, a second terminal coupled to the second voltage and a control terminal coupled to the control signal;

an eighth transistor comprising a first terminal coupled to the first voltage, a control terminal coupled to the second node, and a second terminal;

a ninth transistor comprising a first terminal coupled to the second terminal coupled to the eighth transistor, a control terminal coupled to the control terminal of the first transistor, and a second terminal; and

a tenth transistor comprising a first terminal coupled to the second terminal of the ninth transistor, a control terminal coupled to the control signal and a second terminal coupled to the second voltage.

9. A flipflop, comprising:

a sense amplifier receiving two input signals and outputting complementary latch signals, comprising:

a first latch unit coupled between the common node and a first voltage, comprising a first inverter and a second inverter cross-coupled to each other, and comprising a first node and a second node to output the complementary latch signals respectively; and

a differential pair comprising a first transistor and a second transistor, connected to the first latch unit in parallel, wherein control terminals of the first and second transistors are coupled to the two input signal respectively;

a signal amplification circuit comprising two input terminals coupled to the first node and the second node respectively, a first control terminal

coupled to a control signal, and two output terminals; and

a second latch unit comprising a third node and a fourth node coupled to the two output terminals of the signal amplification circuit.

10. The flipflop as claimed in Claim 9, wherein, in the first latch unit, the first inverter comprises an input terminal coupled to an output terminal of the second inverter, serving as the second node, and an output terminal coupled to an input terminal of the second inverter, serving as the first node.

11. The flipflop as claimed in Claim 10, wherein, in the differential pair, the first and second transistors comprise first terminals coupled to the first node and the second node of the first latch unit respectively and second terminals coupled to a common node together.

12. The flipflop as claimed in Claim 11, wherein the differential circuit further comprises:

a third transistor coupled between the first voltage and the first node of the first latch unit, and comprising a control terminal coupled to the control signal; and

a fourth transistor coupled between the first voltage and the second node of the first latch unit, and comprising a control terminal coupled to the control signal.

13. The flipflop as claimed in Claim 12, further comprising a current source transistor coupled between the

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common node and a second voltage, and comprising a control terminal coupled to the control signal.

14. The flipflop as claimed in Claim 12, wherein the second latch unit comprises:

a third inverter comprising an input terminal and an output terminal; and

a fourth inverter cross-coupled to the third inverter, comprising an input terminal coupled to the output terminal of the third inverter, serving as the fourth node, and an output terminal coupled to the input terminal of the third inverter, serving as the third node.

15. The flipflop as claimed in Claim 14, wherein the signal amplification circuit comprises:

a fifth inverter coupled to the first voltage, comprising an input terminal coupled to the first node and an output terminal coupled to the third node;

a fifth transistor comprising a first terminal coupled to the fifth inverter, a control terminal coupled to the control terminal of the second transistor, and a second terminal;

a sixth transistor comprising a first terminal coupled to the second terminal of the fifth transistor, a second terminal coupled to the second voltage, and a control terminal coupled to the control signal;

a sixth inverter coupled to the first voltage, comprising an input terminal coupled to the second node and an output terminal coupled to the fourth node;

a seventh transistor comprising a first terminal coupled to the sixth inverter, a control terminal coupled to the control terminal of the first transistor, and a second terminal; and

an eighth transistor comprising a first terminal coupled to the second terminal of the seventh transistor, a control terminal coupled to the control signal, and a second terminal coupled to the second voltage.

16. The flipflop as claimed in Claim 14, wherein the signal amplification circuit comprises:

a fifth transistor comprising a first terminal coupled to the first voltage, a control terminal coupled to first node, and a second terminal coupled to the third node;

a sixth transistor comprising a first terminal coupled to the second terminal of the fifth transistor, a control terminal coupled to the control terminal of the second transistor, and a second terminal;

a seventh transistor comprising a first terminal coupled to the second terminal of the sixth transistor, a second terminal coupled to the second voltage and a control terminal coupled to the control signal;

an eighth transistor comprising a first terminal coupled to the first voltage, a control terminal coupled to the second node, and a second terminal coupled to the fourth node;

a ninth transistor comprising a first terminal coupled to the second terminal coupled to the eighth

transistor, a control terminal coupled to the control terminal of the first transistor, and a second terminal; and

a tenth transistor comprising a first terminal coupled to the second terminal of the ninth transistor, a control terminal coupled to the control signal and a second terminal coupled to the second voltage.

17. A flipflop, comprising:

a first transistor comprising a first terminal coupled to a first voltage, a second terminal coupled to a first node, and a control terminal;

a second transistor comprising a first terminal coupled to the first node, a control terminal coupled to the control terminal of the first transistor, and a second terminal coupled to a common node;

a third transistor coupled between the first voltage and the first node;

a fourth transistor coupled between the first node and the common node, comprising a control terminal coupled to a first input signal;

a fifth transistor comprising a first terminal coupled to the first voltage, a second terminal coupled to a second node, and a control terminal coupled to the first node;

a sixth transistor comprising a control terminal coupled to the control terminal of the fifth transistor, a first terminal coupled to the second node and the control terminal of the first transistor, and a second terminal coupled to the common node;

a seventh transistor coupled between the first voltage and the second node;

an eighth transistor coupled between the second node and the common node, comprising a control terminal coupled to a second input signal, wherein the first input signal is inverse of the second input signal;

a ninth transistor coupled between the common node and a second voltage, wherein control terminals of the third, seventh and ninth transistors are coupled to a control signal;

a signal amplification circuit comprising two input terminals coupled to the first and second node respectively, a first control terminal coupled to the control terminal, a second control terminal and a third control terminal respectively coupled to the second and first input signals, a first output terminal and a second output terminal;

a first inverter comprising an input terminal coupled to the first output terminal of the signal amplification circuit, and an output terminal; and

a second inverter comprising an input terminal coupled to the second output terminal of the signal amplification circuit, and an output terminal coupled to the output terminal coupled to the output terminal of the first inverter.

18. The flipflop as claimed in Claim 17, the signal amplification circuit comprising;

a tenth transistor comprising a first terminal coupled to the first voltage, a control terminal coupled

to the first node, a second terminal as the first output terminal coupled to the input terminal of the first inverter;

an eleventh transistor comprising a first terminal coupled to the second terminal of the tenth transistor, a control terminal coupled to the control terminal of first node, and a second terminal;

a twelfth transistor comprising a first terminal coupled to the second terminal of the eleventh transistor, a control terminal coupled to the second input signal, and a second terminal;

a thirteenth transistor coupled between the second terminal of the twelfth transistor and the second voltage;

a fourteenth transistor comprising a first terminal coupled to the first voltage, a control terminal coupled to the second node, and a second terminal as the second output terminal coupled to the input terminal of the second inverter;

a fifteenth transistor comprising a first terminal coupled to the second terminal of the fourteenth transistor, a control terminal coupled to the second node, and a second terminal;

a sixteenth transistor comprising a first terminal coupled to the second terminal of the fifteenth transistor, a control terminal coupled to the first input signal, and a second terminal; and

a seventeenth transistor coupled between the second terminal of the sixteenth transistor and the second voltage, control terminals of the thirteenth and seventeenth transistors, as the first control terminal of the signal amplification circuit, coupled to the control terminal.

19. The flipflop as claimed in Claim 17, the signal amplification circuit comprising:

a tenth transistor comprising a first terminal coupled to the first voltage, a control terminal coupled to the first node, and second terminal as the first output terminal coupled to the input terminal of the first inverter;

an eleventh transistor comprising a first terminal coupled to the second terminal of the tenth transistor, a control terminal coupled to the second input signal, and a second terminal;

a twelfth transistor coupled between the second terminal of the eleventh transistor and the second voltage;

a thirteenth transistor comprising a first terminal coupled to the first voltage, a control terminal coupled to the second node, and a second terminal as the second output terminal coupled to the input terminal of the second inverter;

a fourteenth transistor comprising a first terminal coupled to the second terminal of the thirteenth transistor, a control coupled to the first input signal, and a second terminal; and

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a fifteenth transistor coupled between the second terminal of the fourteenth transistor and the second voltage, control terminals of the twelfth and fifteenth transistors, as the first control terminal of the signal amplification circuit, coupled to the control signal.